**ECE 501 : Contemporary Digital Systems and VHDL**

**Assignment – 2 : Use of QUARTUS Graphic input**

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1. Objective : To use the Quartus to build a circuit (graphic input) for the function,

F = A’B’C’ + A’BC’ + AB’C’ + ABC.

Also to obtain simulation results for all possible values.

1. Design Specification and structure :

* Inputs :

A, B, C are the inputs .Total number of input values for each is 2^3=8 bits.

* Outputs :

C

B

A

A 8 bit function ‘F’ .

* Functional behavior :

F = A’B’C’ + A’BC’ + AB’C’ + ABC.

A’B’C’ + A’BC’ + AB’C’ + ABC

Generates an output –F .

* Timing:

Operates asynchronously.

* Other considerations :

F

None.

1. Design Structure :

Inputs are A ,B , C and the output F is F = A’B’C’ + A’BC’ + AB’C’ + ABC. This function has the following truth table .

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **F** |
| 0 | 0 | 0 | **1** |
| 0 | 0 | 1 | **0** |
| 0 | 1 | 0 | **1** |
| 0 | 1 | 1 | **0** |
| 1 | 0 | 0 | **1** |
| 1 | 0 | 1 | **0** |
| 1 | 1 | 0 | **0** |
| 1 | 1 | 1 | **1** |

Table 2.1 : Truth table

1. Design Entry :

* Circuit ( RTL Viewer and schematic block diagram)

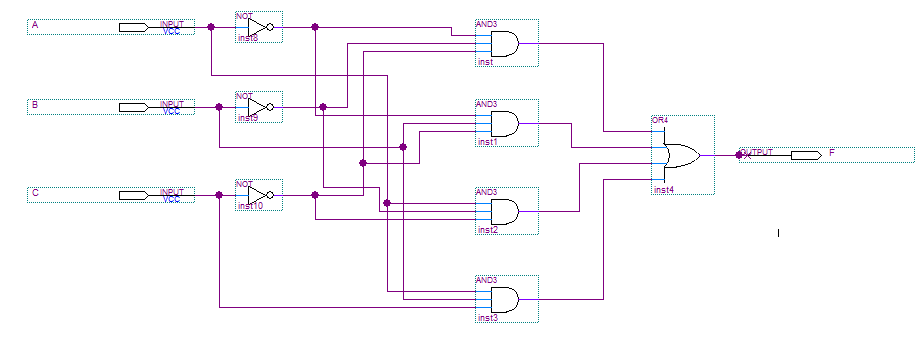


Fig 2.1 : Schematic circuit

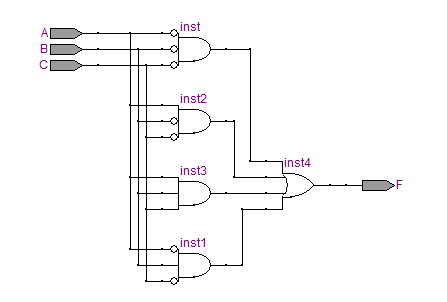
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Fig 2.2 : RTL Viewer

In this circuit , 4 AND logic units are used with one OR gate. The F resembles the function. Three inputs are used. Corresponding, three NOT gates are also used.

* Compilation report :

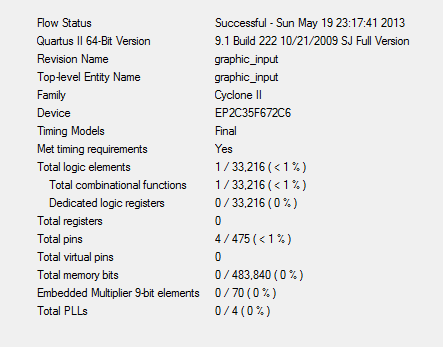
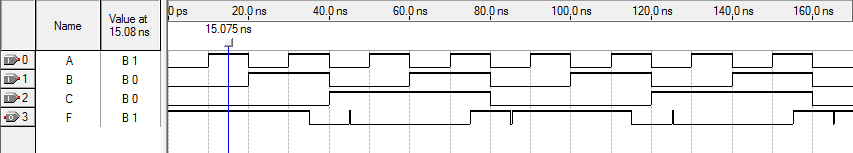


Fig 2.3 : Compilation report

* Simulation report :



These are the glitches

The truth table is satisfied as A=0, B=0, C=1 , F=0

Fig 2.4 : Simulation report

* Design verification plan :

1. Verification by testing the simulation.
2. All input combinations for A,B,C are applied.
3. Verify that outputs correspond to Full Adder Truth Table.
4. Input selected values of A,B and C .
5. Verify their respective outputs corresponding to the truth table.

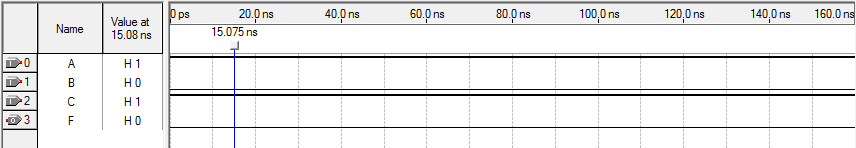


Fig 2.5 : Verification of the truth table

Here A= 1 , B=0, C=1 therefore we obtain F=0 . ( Setting specific value for the test)